ABSTRACT

In view of the transistor off leakage increasing with device miniaturization, the invention provides a semiconductor integrated circuit capable of high-speed readout by eliminating the need for a charge replenishing transistor formerly required to hold a bit line at the "H" level, and thereby speeding up readout of stored data that causes the bit line to transition to the "L" level. To achieve this, a high-potential source line and a low-potential source line are provided. Then, the source of a memory cell is selectively connected to either the high-potential source line and the low-potential source line. In the case of stored data that causes the bit line potential to be held at the "H" level during readout, the source of the memory cell is connected to the high-potential source line, while in the case of stored data that causes the bit line potential to drop to the "L" level during readout, the source of the memory cell is connected to the low-potential source line.